1. A method for fabricating a multilayer ceramic substrate comprising the steps of:

(a) manufacturing an intaglio plate of flexible resin substance, on which a first groove corresponding to a first conductive pattern is formed and a second groove having a depth deeper than that of the first groove is formed at a place corresponding to a via of the first conductive pattern;

(b) filling the first and second grooves with an electroconductive paste, and deaerating and drying the paste;

(c) repeating the cycle of refilling additional electroconductive paste to replenish a volume corresponding to a decrement caused by the drying, and deaerating and drying;

(d) gluing said intaglio plate onto a ceramic substrate by applying heat and pressure;

(e) separating said intaglio plate from said ceramic substrate to have a pattern of the electroconductive paste transferred onto the ceramic substrate, and burning it so as to form said first conductive pattern on the ceramic substrate;

(f) forming an insulation layer on said first conductive pattern; and

(g) forming a second conductive pattern on said insulation layer.

2. The method for fabricating a multilayer ceramic substrate recited in claim 1, wherein said ceramic substrate is provided with a resin layer not thicker than 20 $\mu$ m on at least one surface, said resin being one of a thermosetting resin and a thermoplastic resin.

3. The method for fabricating a multilayer ceramic substrate recited in claim 1, wherein said insulation layer is formed by a printing technology covering the whole area of said first conductive pattern, and said via is exposed through abrasion or grinding of the dried skin of said insulation layer before burning said insulation layer.

4. The method for fabricating a multilayer ceramic substrate recited in claim 1, wherein said insulation layer is formed by a printing technology

covering the whole area of said first conductive pattern, and said via is exposed through abrasion or grinding of said insulation layer after burning said insulation layer.

5. The method for fabricating a multilayer ceramic substrate recited in claim 1, wherein said insulation layer is formed by a printing technology covering the whole area of said first conductive pattern, and said via is exposed through abrasion or grinding of the dried skin of said insulation layer, and then the abrasion or grinding is applied again after burning.

6. The method for fabricating a multilayer ceramic substrate recited in claim 1, wherein said second conductive pattern is formed through the same process steps used for forming said first conductive pattern.

7. The method for fabricating a multilayer ceramic substrate recited in either claim 1 or claim 6, further comprising the step of forming a third conductive pattern and a fourth conductive pattern by the same process step used for forming said first and second conductive patterns on a surface of said ceramic substrate opposite to the surface on which said first and second conductive patterns are formed.

8. The method for fabricating a multilayer ceramic substrate recited in claim 7, in which said first to fourth conductive patterns are formed through a transfer printing technology, wherein the gluing operation for said third conductive pattern and that for said first conductive pattern, and the gluing operation for said fourth conductive pattern and that for said second conductive pattern, respectively, are performed simultaneously.

9. The method for fabricating a multilayer ceramic substrate recited in claim 1, further comprising the step of forming a dielectric layer on a part of said ceramic substrate.

10. The method for fabricating a multilayer ceramic substrate recited in claim 1, wherein a through hole is provided in said ceramic substrate, and said through hole is filled with an electroconductive substance, and then the electroconductive substance is burned.

11. The method for fabricating a multilayer ceramic substrate recited in either claim 1 or claim 6, further comprising the step of mounting an LSI chip with the face down on a part of one of said first and second conductive patterns to be electrically connected.

12. The method for fabricating a multilayer ceramic substrate recited in either claim 1 or claim 6, further comprising the step of mounting an LSI chip with the face down on a part of one of said first and second conductive patterns to be electrically connected, after forming a fine bump on one of said first conductive pattern and said second conductive pattern by disposing said second groove at a place corresponding to a pad of said LSI chip and applying an electroconductive paste on the top of said bump.

13. A multilayer ceramic substrate comprising:

a ceramic substrate;

a first conductive pattern having a convex via, being formed on said ceramic substrate by a transfer printing technology through an intaglio printing using a flexible resin substance;

an insulation layer formed on said first conductive pattern; and

a second conductive pattern electrically connected by way of said via.

14. A multilayer ceramic substrate comprising:

a ceramic substrate;

a first conductive pattern and a third conductive pattern each having a convex via, being formed on said ceramic substrate by a transfer printing technology through an intaglio printing using a flexible resin substance;

an insulation layer formed respectively on said first and third conductive patterns; and

a second conductive pattern and a fourth conductive pattern each electrically connected with said first conductive pattern and said third conductive pattern, respectively, by way of said via.

15. The multilayer ceramic substrate of either claim 13 or claim 14, wherein a meshed pattern is provided in a part of said conductive pattern.

16. The multilayer ceramic substrate of either claim 13 or claim 14, wherein a shield pattern is provided at an outer edge of said conductive pattern.

17. The multilayer ceramic substrate of either claim 13 or claim 14, wherein said ceramic substrate is provided with a through hole filled with an electroconductive substance and burned, and said via is disposed on the through hole.

18. The multilayer ceramic substrate of either claim 13 or claim 14, further comprising a dielectric layer formed on a part of said ceramic substrate.

19. The multilayer ceramic substrate of either claim 13 or claim 14, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected.

20. The multilayer ceramic substrate of either claim 13 or claim 14, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through an electroconductive paste applied on the top of a fine bump provided on one of said first and second conductive patterns, said fine bump formed by using a second groove which is disposed on said intaglio at a place corresponding to a pad of said LSI chip.

21. The multilayer ceramic substrate of either claim 13 or claim 14, further comprising an LSI package mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through a lattice of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said first and second conductive patterns.